0011-00-16-11-000
ZICM35xSP2-1C External Antenna Implementation

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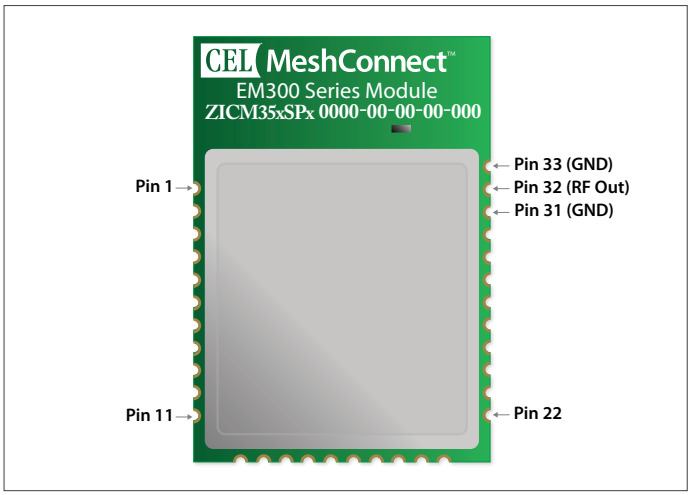

INTRODUCTION

This Technical Note describes the host board layout requirements for using an external antenna with the MeshConnect™ ZICM35xSP2-1C Module from California Eastern Laboratories (CEL). This module has been certified for use with an external antenna through the use of the ZICM35xSP2-1C castellation pin, a U.FL connector and a U.FL cable assembly with a Nearson whip antenna. This document details the implementation required to obtain the regulatory certification. This implementation is applicable to any host board provided the implementation follows the requirements presented in this document.

The RF signal is routed to castellation pin 32 on CEL Part Number ZICM35xSP2-1C. The module has castellation pins 31 and 33 connected to ground to provide the ability to implement a 50Ω co-planer transmission line on a standard two layer FR4 printed circuit board with a thickness of 0.062 inches.

COPLANAR WAVEGUIDE

The coplanar with ground plane waveguide structure consists of the RF trace on the topside of the printed circuit board with adjacent ground planes spaced close to the RF transmission line. A ground plane under the RF trace should also exist directly below the transmission line.

Since the module castellation pad is 40 mils wide on the bottom of the module, an RF trace width of 40 mils, along with a gap of 8 mils separation from the ground plane, will result in a good 50Ω transmission line. Using the transmission line width equal to the castellation pad width eliminates any RF discontinuity which could degrade the return loss.

Figures 1 and 2 below detail the Gerber layout. The transmission line is 40 mils wide with an 8 mil gap to the ground. The length of the transmission line is 200 mils long from the castellation pad to the edge of the U.FL connector. Figure 1 below represents the top layer, while Figure 2 is the bottom layer on the two layer FR4 printed circuit board.

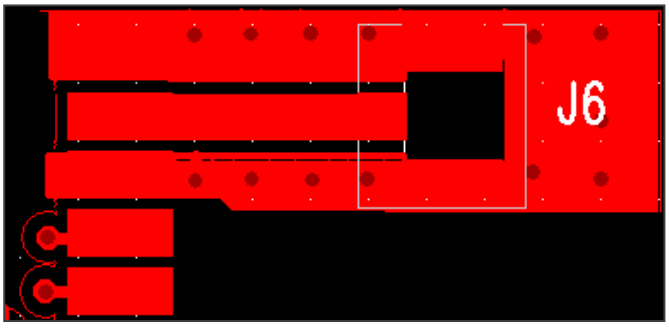

Figure 1. Top Layer

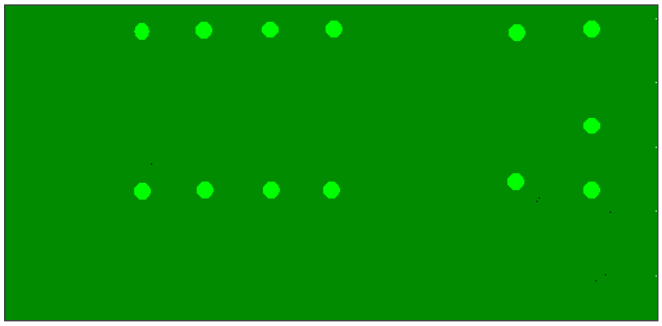

Figure 2. Bottom Layer

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COMPONENTS USED IN THE IMPLEMENTATION

The following components specify the requirements for this implementation:

- CEL Module Part Number: ZICM35xSP2-1C
- U.FL Connector Part Number: U.FL-R-SMT(10) from Hirose Electric Co. Ltd.
- External Antenna: Nearson S181AH-2450S Half-Wave Dipole
- Host Board: FR4 two layer, 0.062" thick with dielectric constant of 4.2 typical. The transmission line between the module and the U.FL connector should be a straight line with a width of 40 mils, and ground plane spaced 8 mils apart on the top layer. The bottom layer should be a continuous ground plane under the transmission line. Ground vias should be included between the module castellation pins and the U.FL connector ground pads to provide a good RF ground connection.
- Cable assembly between the U.FL connector on the host board and the Nearson whip antenna must be a minimum of four inches in length.

Figure 3 below illustrates the implementation.

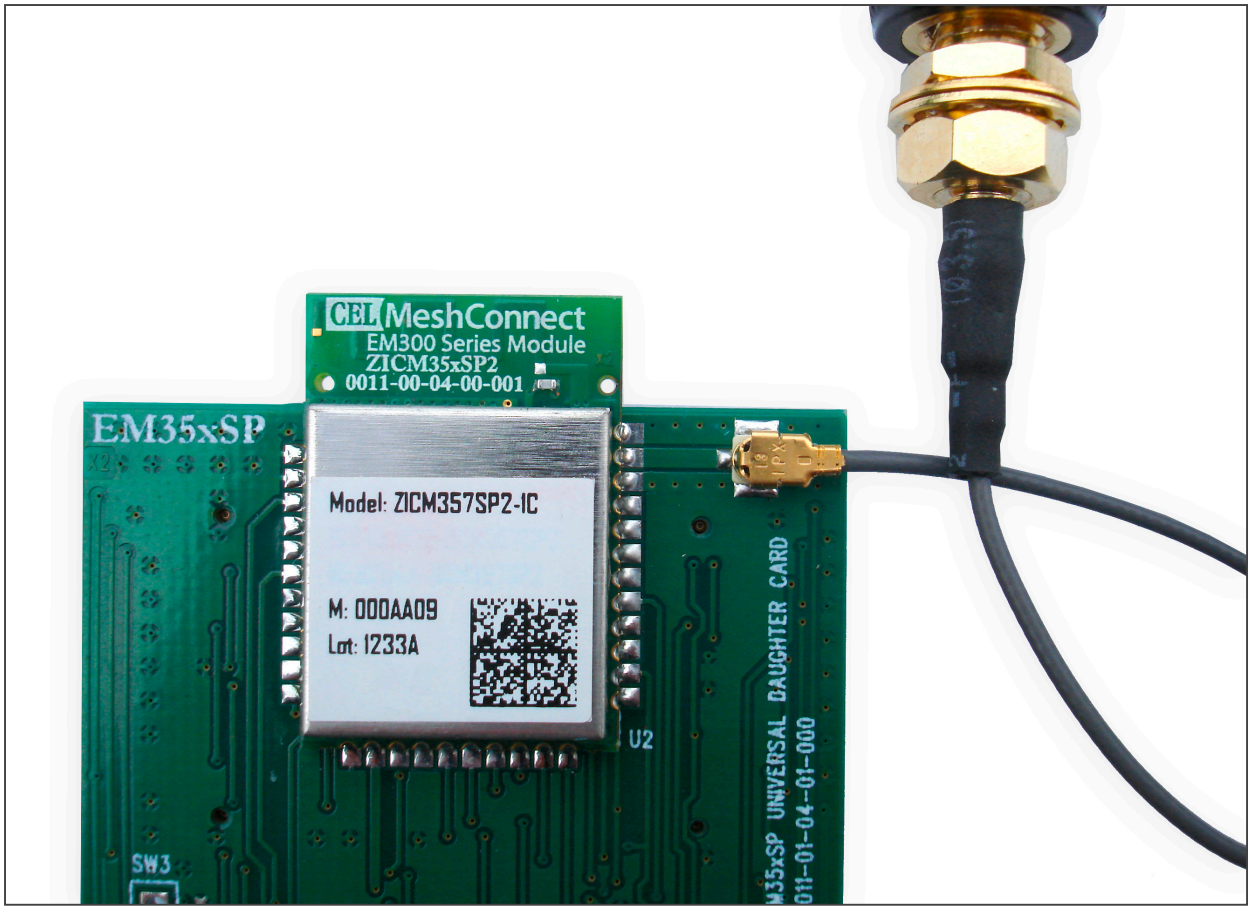

Figure 3. Implementation using connector, cable and external antenna

DESIGN VERIFICATION TEST PROCEDURE

Any manufacturer that chooses to implement the external antenna on their host board should verify that the implementation was done properly. To assist with this, the following Test Procedure can be used. The procedure uses a Network Analyzer capable of making return loss measurements at 2.4 GHz.

1. Calibrate the network analyzer for a one port measurement with a center frequency of 2.44 GHz and a span of 200 MHz.
2. Take a blank host board and solder a 100 Ω resistor between castellation Pin 31 and 32.
3. Solder a second 100 Ω resistor between castellation Pin 32 and 33.
4. Solder the U.FL connector on the host board.
5. Using the appropriate U.FL to SMA adapter for your network analyzer, measure the Return Loss of the trace, (either S11 or S22 depending on which port was chosen during the 1-port calibration).
6. A return loss of -15 dB or lower indicates an acceptable implementation (PASS).

Figure 4 displays the measurement where Port 2 was used as the measurement Port.

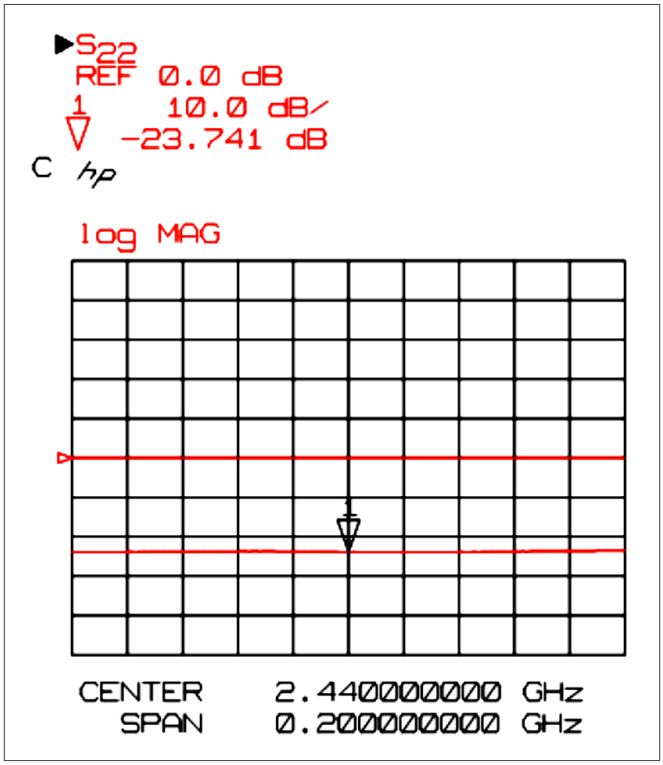

Figure 4. Measured Return Loss of RF trace

PRODUCTION TEST PROCEDURE FOR ENSURING COMPLIANCE

During production, host boards should be tested to ensure compliance. CEL recommends that when the host board is manufactured, the requirement of “Electrical Testing” is specified with the PCB order to guarantee that no short is present anywhere on the host board (which includes the trace between the U.FL connector location and the module RF castellation pad). This greatly simplifies the production test requirements down to verifying that a solder short did not occur during the component placement and reflow of the host board assembly. Verifying no solder short has occurred can be done by measuring an open circuit between castellation pins 32 and 33 using a DC multi-meter.

REFERENCES

Reference Documents	Download
California Eastern Laboratories	
0011-00-07-00-000 CEL – EM357 Mini Modules Datasheet	Link

REVISION HISTORY

Previous Versions	Changes to Current Version	Page(s)
0011-00-16-11-000 (Issue A) August 26, 2013	Initial Technical Note	N/A

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